

UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE

Department of Electrical Engineering

Experiment No. _____ Transistor Biasing

INTRODUCTION

Two important considerations when biasing a transistor are (1), Quiescent conditions and, (2) temperature stability. For the biasing network in Figure 1 (and its equivalent in Figure 2), the temperature stability factor can be expressed by the following equation:

$$S = \frac{\partial}{\partial I_{CO}} I_C = \frac{(1 + \beta_{DC})(R_B + R_E)}{R_B + (1 + \beta_{DC})R_E}$$

where,

I_C - collector current

I_{CO} - reverse saturation current

β_{DC} - DC forward current transfer ratio

R_B - base-current biasing resistor

R_E - temperature stabilization resistor

The resistor, R_E , basically senses any changes in the collector current due to temperature changes and feeds it back across the base-to-emitter as a negative voltage which in turn reduces the base current. A reduction in the base current would reduce the amount of change in the collector current.

It is desirable that the stability factor be made to approach one. To do this would require that R_E be much larger than R_B , which in turn needs to be large for biasing purposes. A large value of R_E would require that the supply voltage be large in order to maintain a reasonable quiescent condition. This would be impractical and so it becomes a matter of compromise. Generally the stability factor is chosen to be somewhere between 5 and 10 and the resistor, R_E , so as to have a DC bias voltage across it equal to about one-third of the power supply voltage.

$$R_E = \frac{V_{CC}}{3 I_{CQ}}$$

$$R_B = \frac{(S - 1)(1 + \beta_{DC})R_E}{1 + \beta_{DC} - S}$$

Generally, quiescent conditions are chosen with certain desirable results in mind, i.e., maximum gains, maximum input-output signal levels, maximum efficiency, etc. With the desired result in mind and a set of characteristic curves, the biasing parameters can be readily obtained. For this experiment, maximum signal levels for a common-emitter, Class A amplifier are of interest.

Before constructing the DC load-line on the output characteristic curves, the power supply, VCC, must be specified. Since it is desirable to obtain maximum signal levels, the power supply voltage should be made approximately VCEmax, the DC load-line should be at or just below the maximum power curve, and the collector bias voltage, VCE-Q, should be made approximately one-third the supply voltage.

$$V_{CE-Q} = V_{CC}/3 = V_{CEmax}/3$$

This in effect permits the AC signal to swing an equal amount about the quiescent point with a minimum of distortion.

With the VCE-Q known, IC-Q and IB-Q can be determined directly from the curves and the DC load-line. The transistor parameter, β_{DC} , can be determined at the quiescent point.

$$\beta_{DC} = I_{C-Q}/I_{B-Q}|_{V_{CE-Q}}$$

The DC voltage equation about the collector-emitter side of the transistor in Figure 2 can be written as follows:

$$V_{CC} = (R_C \times I_{C-Q}) + V_{CE-Q} + R_E(I_{C-Q} + I_{B-Q})$$

The base current, IB-Q, is generally very small compared with the collector current, IC-Q, and can be neglected. The above equation written first in terms of VCE-Q and then in terms of IC-Q becomes;

$$V_{CE-Q} = V_{CC} - (R_C + R_E)I_{C-Q}$$

$$I_{C-Q} = (V_{CC} - V_{CE-Q})/(R_C + R_E)$$

The two ends of the DC load-line can be identified by first letting

$$I_C = 0 \text{ and then } V_{CE} = 0.$$

$$V_{CEmax} = V_{CC}|_{I_C=0}$$

$$I_{Cmax} = V_{CC}/(R_C + R_E)|_{V_{CE}=0}$$

The slope of the DC load-line = $I_{Cmax}/V_{CEmax} = 1/(R_C + R_E)$
or,

$$R_C = (V_{CC}/I_{Cmax}) - R_E$$

The equivalent circuit of Figure 2 is obtained by determining the Thevenin's equivalence of the base circuit looking back from the input to the transistor. The Thevenin's equivalent resistance, R_B , and Thevenin's equivalent voltage, V_{BB} , would be as follows:

$$R_B = (R_1 \times R_2)/(R_1 + R_2)$$

$$V_{BB} = [R_2/(R_1 + R_2)]V_{CC} = [(R_1 \times R_2)/(R_1 + R_2)]V_{CC}/R_1$$

$$V_{BB} = (R_B/R_1)V_{CC}$$

The DC voltage equation about the equivalent base circuit in Figure 2 can be written as follows:

$$(R_B/R_1)V_{CC} = (R_B + R_E)I_{B-Q} + V_{BE-Q} + (R_E \times I_{C-Q})$$

The circuit elements, R_1 and R_2 , can now be determined.

$$R_1 = (R_B \times V_{CC})/[(R_B + R_E)I_{B-Q} + V_{BE-Q} + (R_E \times I_{C-Q})]$$

$$R_2 = (R_B \times R_1)/(R_1 - R_B)$$

As a note of interest, for the circuits of Figure 1 through 3, the capacitors will look like open-circuits to DC signals and short circuits to AC signals. Also, the DC power supply will look like a short-circuit to AC signals.

The purpose of this experiment is to gain an understanding of the techniques used in biasing a transistor as a Class A common-emitter amplifier.

PRELIMINARY

P-1. Obtain from the manufacturer's specifications the absolute maximum values of the parameters listed below for the 2N3904 (or its equivalent).

Collector-Base Voltage, V_{CBO} : _____ 60V _____.
Collector-Emitter Voltage, V_{CEO} : _____ 40V _____.
Emitter-Base Voltage, V_{EBO} : _____ 6V _____.
Continuous Collector Current: _____ 200 μ A _____.
Continuous Power Dissipation @ 25 C: _____ 310mA _____.

Also sketch the pin-out configuration of the transistor:

REFER MANUAL FOR pin diagram

P-2. Obtain a set of common-emitter output characteristic curves for the transistor of Procedure P-1 above (either from a curve tracer or from a previous experiment). Bias the transistor as described in the Introduction above, specifying quiescent conditions and determining all the external element values.

Refer pg.130 chapter 5. Transistor Characteristics

Integrated electronics (Analog and digital circuits and systems)

Jacob Millman & Christos C.Halkias

P-2. (Cont.)

INSTRUCTOR'S SIGNATURE _____ DATE _____

Suggested Reference

chapter 5. Transistor Characteristics

Integrated electronics (Analog and digital circuits and systems)

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PROCEDURE

- F-1. Connect the circuit of Figure 1 using parameters calculated in the Preliminary exercise above. Vary R_1 , if necessary, to obtain a $V_{CE-Q} = V_{CC}/3$. Record any changes in R_1 .
- F-2. Apply the circuit of Figure 3 to the input of the amplifier of Figure 1. Set the frequency of the sinusoidal signal source to 5 K-Hertz. Using a dual-trace oscilloscope, increase the magnitude of input signal, e_s , until the output, e_o , begins to distort. Record the peak-to-peak values of e_s , e_i , and e_o .

REPORT

- R-1. Determine the input current, i_s , of the transistor amplifier using experimental data.

$$i_s = (e_s - e_i)/100,000$$

- R-2. Determine the output current, i_o , of the transistor amplifier using experimental data.

$$i_o = e_o/R_C$$

- R-3. Determine the voltage gain, A_v , and current gain, A_i , of the amplifier using experimental data.

$$A_v = e_o/e_i$$

$$A_i = i_o/i_s$$

- R-4. Determine the input impedance of the transistor amplifier, Z_i , the input impedance of the transistor, Z_t , and the current into the base of the transistor.

$$Z_i = e_i/i_s$$

$$Z_t = (Z_i \times R_B)/(R_B - Z_i)$$

$$i_b = (Z_i/Z_t)i_s$$

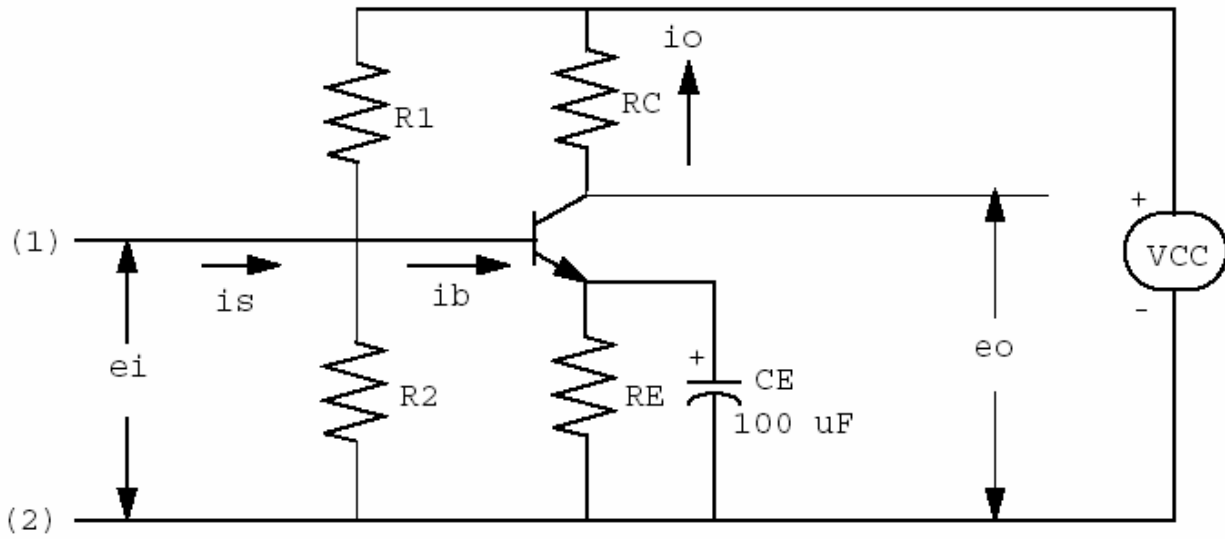


Figure 1.

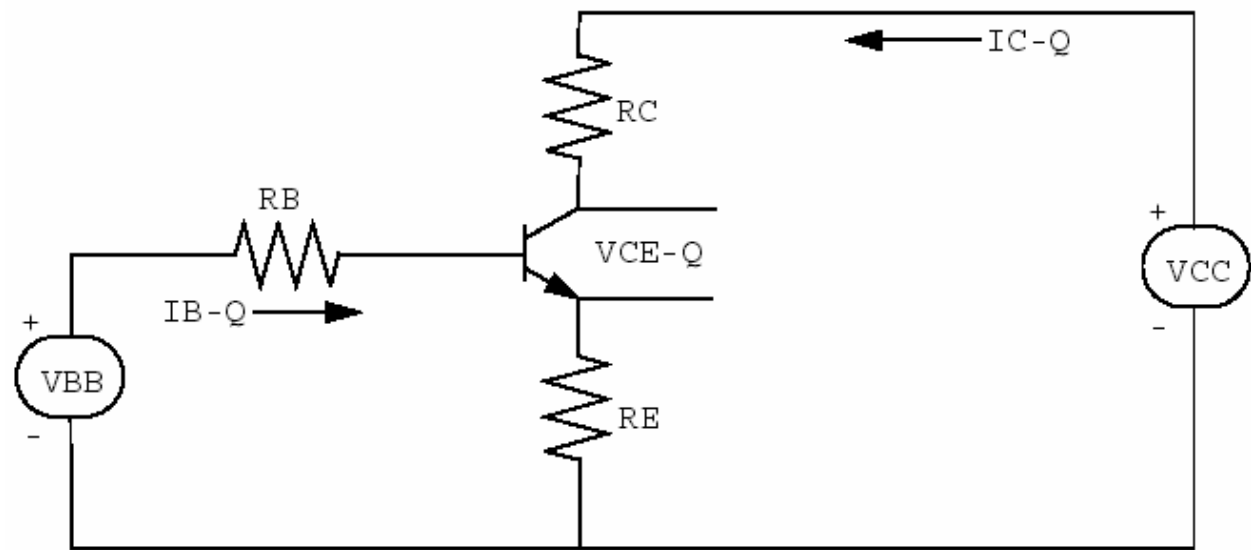


Figure 2.

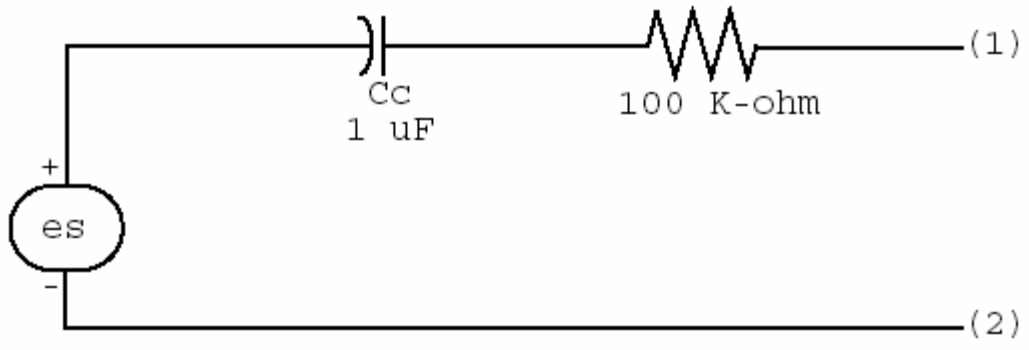


Figure 3.

NOTE: REVERSE THE POWER SUPPLY POLARITY (VCC) AND THE POLARIZED CAPACITOR POLARITY IF THE TRANSISTOR IS A PNP!